GOR Gesellschaft für Operations Research e.V.

Joseph-Sommer-Straße 34, 41812 Erkelenz, Tel.: 02431 9026710, Fax: 02431 9026711

GOR-Arbeitsgruppe: Praxis der Mathematischen Optimierung

Prof. Dr. Josef Kallrath,
Am Mahlstein 8
D-67273 Weisenheim am Berg
Tel: +49 172 747-0689
Fax: +49 621 60-6678297

Herewith we would like to invite you to the 92nd meeting of the GOR working group "Real World Mathematical Optimization" at Infineon Technologies AG (www.infineon.com) in Regensburg, Germany. This meeting is hold as a symposium with the topic

Mathematical Optimization in the Semiconductor Industry

The workshop takes place on April 3rd and 4th in 2014.

The working language will be preferably English, since some speakers are expected from abroad.

Please note that the participation in a GOR-AG-Workshop for non-members is subject to a registration fee, unless you are a speaker or a host.

The latest information on the meeting is available on the homepage of the GOR (https://gor.uni-paderborn.de/index.php?id=224).

Yours sincerely,

Josef Kallrath (GOR AG) & Steffen Rebennack (Colorado School of Mines) & Hermann Gold (Infineon Technologies AG)

GOR Gesellschaft für Operations Research e.V.

Mathematical Optimization in the Semiconductor Industry

The Infineon Technologies AG offers semiconductor and system solutions, addressing three central challenges to modern society: energy efficiency, mobility and security. With around 26,700 employees worldwide, the company achieved a turnover of 3.9 billion Euros in fiscal 2012 (ending September). The company is listed in Frankfurt under the symbol "IFX" and in the U.S. over the counter market OTCQX International Premier under the symbol "IFNNY".

As a global company and a world leader in its target markets, Infineon Technologies AG offers semiconductor and system solutions for automotive, industrial electronics, chip card and security applications. The plant in Regensburg is innovation and high-tech factory production site combined. There, Infineon develops and manufactures semiconductor products with about 2,000 employees.

Sensors for automotive applications are as much a product portfolio as microcontroller for industrial applications, the intelligent interior of smart cards and electronic passports or chips for consumer electronics. For example, our high-tech chip solutions make paying with the credit card safe, help in air conditioning systems and electric drives to save electricity and eject, just in case, the side airbag in fractions of a second. Around the world, innovative products from Regensburg ensure that our lives are a little safer and more comfortable. Additional information can be found at: www.infineon.com .

This two-days event will attempt to give an overview of the current state of the art of mathematical optimization in the Semiconductor Industry. Please contact

Dr. Hermann Gold
Infineon Technologies AG
IFAG OP FE OPC IE ORE
Tel.: +49 941 202 1466
Fax.: +49 941 202 941466
Mobile: +49 160 531 9394
e-mail: hermann.gold@infineon.com,

Steffen Rebennack or myself if you are interested in presenting.

In talks, each approx. 40 minutes experts from practice, research institutions or software companies, will present selected problems and the corresponding solutions

Accommodation:

The Best Western Premier Hotel is located close to the conference venue, the production plant of Infineon in Regensburg. There is a good connection from the hotel to the conference via public transportation.

Address:

Ziegetsdorfer Str. 111
93051 Regensburg, Germany
Tel.: +49 941 463930
Fax.: +49 941 46393400

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92. Meeting of the GOR Working Group
„Real World Mathematical Optimization“

Mathematical Optimization in the Semiconductor Industry

Infineon Technologies AG, Regensburg, April 3 & 4, 2014

Thursday, April 3 - 2014: 09:30 – 22:00

09:30-09:40 **Opening and Welcome** (J. Kallrath & S. Rebennack & H. Gold)

09:40-10:00 **Lutz Labs** (Senior Director, Infineon, Regensburg, Germany)
Greetings, Welcome and Overview on Infineon

10:00-10:40 **Dr. Hermann Gold** (Infineon, Regensburg, Germany)
Activity Analysis in Semi-Conductor Manufacturing: Part I

10:40-11:00 ---------- Coffee Break ----------

11:00-11:40 **Dipl.-Math. Jan Schneider** (University of Bonn, Bonn, Germany)
Transistor-Level Layout of CMOS Cells

11:40-12:20 **Dr. Monica Rafaila** (Infineon, Neubiberg, Germany)
Optimization in Product Design and Development

12:20-12:30 ----- Taking a Group Photograph for the Press -------

12:30-13:45 ---------- Lunch Break ----------

13:45-14:00 **Dr. Hermann Gold** (Infineon, Regensburg, Germany)
Activity Analysis in Semi-Conductor Manufacturing: Part II

14:00-14:40 **Prof. Dr. Josef Kallrath** (GOR Arbeitsgruppe, Weisenheim am Berg) &
Prof. Dr. Steffen Rebennack (Colorado School of Mines, Golden, USA)
Column Enumeration and Generation for Machine Assignment in the Semiconductor Industry

14:40-15:00 **Dr. Michael Bussieck** (GAMS GmbH, Frechen, Germany)
Decomposition Approaches and Their Implementation in GAMS

15:00-15:20 ---------- Coffee Break ----------

15:20-16:00 **Prof. Dr. Lars Mönch** (University of Hagen, Hagen, Germany)
Using Cycle Time Information in Production Planning Formulations for Semiconductor Wafer Fabrication Facilities

16:00-16:15 **Internal Meeting** of the Working Group

16:15-18:30 ----- Visit & Guided Tour: Keplerwohnhaus in Regensburg --------

18:30 - **Conference Dinner**
Celebrating the 92nd meeting of our GOR Working Group

GOR Gesellschaft für Operations Research e.V.

Friday, April 4 - 2014: 09:45 – 16:00

09:45-10:25 **Christian Schiller** & **Dr. Thomas Ponsignon** (Infineon, Neubiberg)
Modeling and Solving Master Planning Problems in Semiconductor Manufacturing

10:25-11:00 ---------- Coffee Break ----------

11:00-11:40 **Dr. Horst Zisgen** (IBM, Mainz, Germany)
Optimization Kombinierte Warteschlangen- und Optimierungsmodelle für die Planung in der Halbleiterfertigung

11:40-12:20 **Prof. Dr. Siegfried Jetzke** (Ostfalia Hochschule, Salzgitter, Germany)
Wait or not to wait -- a question in logistics and production

12:20-13:45 ---------- Lunch Break ----------

13:45-14:25 **Dr. Sven Peyer** (IBM, Boeblingen, Germany)
Efficient Algorithms in VLSI Routing

14:25-15:05 **Dipl.-Math. Michael Gester** (University of Bonn, Bonn, Germany)
VLSI Routing for Multiple Patterning Technology

15:05-15:45 **Dipl.-Ing. Daniel Tonke** (TU Munich, Munich, Germany)
Transport Modules with Two Independent Arms in Cluster Tools

15:45-16:00 **Final Discussion – End of the Workshop – Coffee Break**

The Speakers

Michael Gester received his Diploma degree in mathematics at the University of Bonn, Germany, in 2009. Since then he is a PhD student and scientific staff member at the Research Institute for Discrete Mathematics, University of Bonn. His current research interests are discrete optimization, computational geometry and its applications in VLSI design, including the development of the VLSI design software BonnTools in cooperation with the industry partner IBM.

Hermann Gold is a Senior Staff Engineer at Infineon Technologies AG, where he is working on planning and scheduling problems in semiconductor manufacturing. He studied computer science at the University of Erlangen and received a doctorate degree from the Faculty of Mathematics at the University of Würzburg. His special research interest is in the combination of queueing theory and optimization.

Siegfried Jetzke is professor for *Technische Grundlagen und Logistik* at the *Ostfalia Hochschule für angewandte Wissenschaften* in Salzgitter and head of *good*Sync, a small company developing software for simulation and optimization for logistics and production. He studied physics and mathematics and received his doctoral degree in theoretical physics with a work on non - linear processes in laser - atom - interactions. Before becoming engaged in logistics he worked non - linear optics, simulation and optimization problems in genetics as well as transportation problems of nuclear particles. Nowadays he feels to be positioned between the practitioner in production or logistics and the theoretician.

Necip Baris Kacar is an Operations Research Specialist at the SAS Institute. He holds a Ph.D. degree in Industrial Engineering with Minor in Operations Research from the Edward P. Fitts Department of Industrial and Systems Engineering at North Carolina State University, and also holds a M.S. from the same university. He received a BS degree in Mechanical Engineering from Bogazici University, Istanbul, Turkey. His research interests are in production planning, supply chain management, inventory optimization and simulation based optimization.

Josef Kallrath obtained his PhD in astrophysics from Bonn University (Germany) in 1989. He is a professor at the University of (Gainesville, FL, www.astro.ufl.edu/∼kallrath), and solves real-world problems in industry using a broad spectrum of methods in scientific computing, from modeling physical systems to supporting decisions processes by mathematical optimization. He has written review articles on the subject, about 100 research papers in astronomy and applied mathematics, and several books on mixed integer optimization, as well as one on eclipsing binary stars.

He leads the Real World Optimization Working Group of the German Operations Research Society. His current research interests are polylithic modeling and solution approaches to solve large-scale or difficult optimization problems, for instance, by decomposition techniques such as column generation, or hybrid methods.

Lars Mönch is a professor of Computer Science at the Department of Mathematics and Computer Science, University of Hagen where he heads the Chair of Enterprise-wide Software Systems. He holds MS and Ph.D. degrees in Mathematics from the University of Göttingen, Germany. After his Ph.D., he obtained a habilitation degree in Information Systems from Technical University of Ilmenau, Germany. His research and teaching interests are in information systems for production and logistics, simulation, scheduling, and production planning.

Sven Peyer received his PhD in mathematics from the University of Bonn (Germany) in 2007. He joined IBM in 2007 and works as an Advisory Development Engineer on algorithmical solutions and methodologies in chip design. His main interest is VLSI routing.

Monica Rafaila works as a researcher at Infineon Technologies AG, supervising PhD and master students projects. She obtained her PhD from Vienna University of Technology in 2010. Her current activities focus on methodologies and algorithms for automation of test planning and data analysis, as well as robustness assessment and optimization, in industrial flows. Examples include circuit-to-system level simulation-based verification, chip-level testing, in the presence of several sources of variations (operating conditions, technological andprocess variations, calibration parameters). Research interests include: experiment planning and statistical analysis, metamodel fitting and optimization, data mining, probability distribution analysis and optimization.

Steffen Rebennack is an Assistant Professor at the Colorado School of Mines, USA. He obtained his PhD at the University of Florida. His research interests are in dimension-reduction techniques for large-scale optimization problems, particularly with applications in power systems, stochastic optimization and global optimization.

Christian Schiller is working as a Senior Staff Engineer in the Corporate Supply Chain organization of Infineon Technologies AG in Munich, Germany. He is responsible for the Production Planning process and related projects. Over the last 4 years, he was introducing a new solver based master planning process at Infineon. It has been used successfully for over one year now. His current focus lies on identification of process and tool improvements in the area of production planning and production scheduling.

Jan Schneider is a PhD student and scientific staff member at the Research Institute for Discrete Mathematics at the University of Bonn, Germany, where he also received his Diploma degree in mathematics in 2009. His current research interests are discrete optimization and its application in VLSI design, including the development of the BonnTools software in cooperation with the institute's industry partner IBM.

Daniel Tonke received an M.S. degree in Industrial and Systems Engineering from KAIST, Daejeon, Korea, and an Dipl.-Ing degree in Industrial Engineering (Wirtschaftsingenieurwesen) from the Technical University Berlin, Berlin, Germany. Currently, he is pursuing his Ph.D. at the Technical University of Munich in the Production and Supply Chain Management research group. His research interests are in the area of production planning in semiconductor and process industries.

Reha Uzsoy is Clifton A. Anderson Distinguished Professor in the Edward P. Fitts Department of Industrial and Systems Engineering at North Carolina State University. He holds BS degrees in Industrial Engineering and Mathematics and an MS in Industrial Engineering from Bogazici University, Istanbul, Turkey. He received his Ph.D. in Industrial and Systems Engineering in 1990 from the University of Florida. His teaching and research interests are in production planning, scheduling, and supply chain management. He was named a Fellow of the Institute of Industrial Engineers in 2005, Outstanding Young Industrial Engineer in Education in 1997, and has received awards for both undergraduate and graduate teaching.

Horst Zisgen ist Leiter einer Entwicklungsabteilung der IBM Deutschland Research und Development GmbH in Mainz. Nach seinem Studium der Mathematik und Informatik an der TU Clausthal promovierte er als Stipendiat der IBM an der Mathematisch-Naturwissenschaftlichen

Fakultät der TU Clausthal über Warteschlangennetzwerke mit Gruppenbedienung. Im Anschluss an die Promotion wechselte er zur IBM, wo er u.a. für die IBM Halbleiterfabrik in East Fishkill das auf Warteschlangennetzwerken basierende Planungs- und Analysetool EPOS als Lead-Architekt leitete. Horst Zisgen ist neben seiner Tätigkeit bei der IBM Lehrbeauftragter am Institut für Angewandte Stochastik und Operations Research der TU Clausthal und Angehöriger des gemeinschaftlichen Simulationswissenschaftlichen Zentrums der Universitäten Göttingen und Clausthal.

VLSI Routing for Multiple Patterning Technology

Michael Gester
Research Institute for Discrete Mathematics, University of Bonn
Lennéstr. 2, 53113 Bonn, Germany
e-mail: gester@or.uni-bonn.de

In *VLSI routing* the basic task is to connect specified circuits on a chip by horizontal and vertical wires on different layers (*Manhattan routing*). For the design of modern computer chips millions of such connections have to be computed in at most few hours run time, in a 3-dimensional grid graph containing hundreds of billions of vertices. The task is complicated by numerous constraints, such as complex geometric design rules or maximum allowed detours for some connections, and competing objective functions, such as minimum (weighted) connection length or wire spreading, to name just a few of them.

Multiple patterning technology is a manufacturing technique for enhancing feature density on a chip by assigning features of a single layer to different production steps.

In this talk we will focus on new challenges in VLSI routing arising from multiple patterning technology. We will present efficient solutions implemented for BonnRoute, a routing tool developed at our institute in cooperation with our industry partner IBM, where it is successfully applied in the VLSI design flow.

Activity Analysis in Semiconductor Manufacturing

Hermann Gold
Infineon Technologies AG
Wernerwerkstr. 2, 93049 Regensburg, Germany
e-mail: hermann.gold@infineon.com

In this talk activity analysis and accompanying optimization to problems arising in semiconductor manufacturing are presented. The areas of application considered are cluster tools and alternate routes as for physical environments, the issue of blocking and synchronization as far as queueing aspects are concerned and the identification of resource pools in view of fairness requirements.

Cluster tools and wet etch benches in semiconductor manufacturing have to be treated by more intricate analysis for scheduling and even for planning than normal single wafer processing tools. This is mainly due to the fact that there is (almost) no queueing allowed for the items, i.e. wafers, for which a certain processing goal has to be achieved. Moreover a given processing goal can be achieved in multiple ways on a given machine. This multiplicity can be thought of as being described by a Boolean expression. Hence the question how to satisfy a set of Boolean expressions in the best way as to fulfill certain efficiency and performance goals has to be answered. The problem of an appropriate normalization of resource consumption has to be tackled in a practical manner. In the end a nominal plan has to be created which leads to load minimality and homogeneity in medium term and feasible schedules at the manufacturing floor. An algebraic modeling and optimization approach for both these issues is presented.

The challenge arising from alternate routes differs from that in cluster tool environments in two aspects. The difficulty with blocking queues is absent (except for time coupling issues) but on the other hand the number of alternatives which are possible in principle may become very large. Mere column enumeration techniques may fail for the analysis and optimization of this type of problems and also for upcoming future cluster tools and improved modeling of todays cluster tools. The necessity to apply the column generation technique is motivated using an example where tasks should be parallelized where possible.

Finally we demonstrate the application of the lexical difference principle to yield a high degree of fairness and resource pooling for the complex machines and processing structures considered.

Wait or not to wait – a question in logistics and production

Siegfried Jetzke
Ostfalia Hochschule für angewandte Wissenschaften
Karl - Scharfenberg - Str. 55 - 57, 38229 Salzgitter
e-mail: s.jetzke@ostfalia.de

Time dependent problems are of great importance for the performance of systems in logistics and production when dealing with delivering goods *on time* but also in synchronizing different processes.

A typical synchronization point is a ramp, where the load of incoming trucks has to be transferred to some warehouse. To illustrate the problem under consideration, think of a production plant with 200 trucks arriving one day and 300 the next day. The numbers are fictitious, but not unrealistic. How can employees manage 300 trucks when they are already busy with 200? How do they spend their idle time when 200 arrive, but they can manage 300? Quite often, the number of employees needed is determined by the peaks observed. A well established solution to this problem in practice is engaging employees for 200 and having some more on standby.

In this talk we will we will present a different approach and address two questions. Is it possible

- to handle different work loads with the same number of employees
- to increase the efficiency without reducing the quality?

To illustrate the idea, consider a warehouse with 100 different storage shelves, arranged linear and material enters and leaves the warehouse at the same place. Incoming orders consist of one or jobs to be processed – articles have to moved to or from the warehouse. Place # 1 is closest to the exit, place # 100 the most distant.

- Obviously it takes more time to pick up an article from place #100 than one from #1.
- If it is possible to take two articles in one batch, the distance that has to be covered is determined by the place most distant from the exit.

¿From this we can infer some very simple conclusions.

- If there is time enough we should go to place #100 and we should go to place #1 when we have to hurry.
- Combining two pairs, e. g. $\mathcal{P}_1(\#3, \#74)$ and $\mathcal{P}_2 = (\#15, \#65)$, of articles would decrease the total distance needed. Considering two pairs independently the total distance $\ell = \ell_1 + \ell_2$ adds up to $\ell = 74 + 65 = 139$. Combining them to $\mathcal{P}_1^*(\#3, \#15)$ and $\mathcal{P}_2^* =$

(#74, #65) gives $\ell^* = 15 + 74 = 89$. If both orders pop up one after another the combination can not be done before the second order is available. i. e. shortening the distance might result in a longer makespan.

In addition, employees having idle time can re - arrange articles.

On arrival of an order, we have to decide

- whether time is short or not – the answer depends on the information available.
- to wait for a next order or orders for combining or not – a problem of optimal stopping
- how can articles be re - arranged – an optimization problem

In addition we must always have in mind that the logistical system is a network, with one linkage caused by the physical flow of goods and another one by data or information. The strength of these linkages will determine strategies and the maximum achievable performance.

One focus of this talk will be how combining of orders can help to increase the performance, determined by efficiency and quality. In the example given above, the total distance is the sum of the distances to the 1^{st} and 3^{rd} job, the probality is given by some joint order statistics. We will give an introduction to the usage of order statistics for improving processes for logistics and production.

Combining even more orders with a larger number of jobs would result in even larger savings but also in additional work, needed to recombine all articles. Waiting too long also means that we might finish too late.

When do we stop waiting? What are different strategies depending on the degree of knowledge of incoming orders. This will be a second focus of this talk.

Having everything lined up linearly calculation of distances is trivial. This changes, when looking at a real live warehouse with several employees. We will discuss some real life constraints and implications and extensions to scheduling problems for processes in production. Given production plans introduce some more knowledge on one hand but decreases the degrees of freedom on the other.

In both cases –logistics and production – waiting does not necessarily mean to *waste time*, waiting can result in gaining time, in many cases in gaining efficiency.

Acknowlegdement:

I thank Dr. B.R.L. Siebert for many helful und fruitful discussions and suggestions.

Column Enumeration and Generation for Machine Assignment in the Semiconductor Industry

Josef Kallrath
GOR Arbeitsgruppe
Praxis der mathematischen Optimierung
Am Mahlstein 8, 67273 Weisenheim am Berg, Germany
e-mail: firstname.lastname@web.de

Steffen Rebennack
Division of Economics and Business
Colorado School of Mines, Golden, CO, USA
www.rebennack.net

We are considering an assignment problem of operations to machines, present in the semiconductor industry. Each machine by itself has a number of chambers. The possible use of these chambers by a given process on a particular machine is given by a Boolean expression. Any true assignment of this Boolean expression yields an alternative way to process an operation on a particular machine. Given arrival rates for each single operation, we seek to minimize the maximum utilization of the resources (*i.e.*, machines) given. This problem can be formulated as a linear programming problem (LP). In the LP, each column represents one true assignment; the LP can be interpreted as a column enumeration approach.

In the real production system, problem instances, contain up to 20 machines with up to 15 chambers and hundreds of operations. This leads to LP problems of several ten million decision variables; the problems are two orders of magnitude too large for current state-of-the-art LP solvers. Thus, we present a column generation algorithm to efficiently solve these instances. The master problems are LPs, while the pricing problems are the optimization variant of the satisfiability problem and as such NP-complete.

Using Cycle Time Information in Production Planning Formulations for Semiconductor Wafer Fabrication Facilities

N. Baris Kacar
SAS Institute
Cary, NC 27513, USA
e-mail: Baris.Kacar@sas.com

Lars Mönch
University of Hagen
Universitätsstraße 1, 58097 Hagen, Germany
e-mail: Lars.Moench@fernuni-hagen.de

Reha Uzsoy
North Carolina State University
Raleigh, NC 27695, USA
e-mail: ruzsoy@ncsu.edu

In this talk, we discuss production planning formulations for semiconductor wafer fabrication facilities (wafer fabs). On the one hand, these formulations require lead time information. On the other hand, the lead time is determined by, and not an input into, the planning process, because the amount of work released into the wafer fab over time determines the resource utilization and hence the cycle times. We consider a finite planning horizon divided into discrete periods of equal length. The objective of the researched production planning model is to determine the amount of each product to release into the wafer fab in each period to maximize the profit. Multiple resource types with limited capacity are considered. Three different ways of considering lead times are discussed:

- lead times that are an integer multiple of the underlying planning period
- fractional lead times based on the formulation of Hackman and Leachman
- non-linear clearing functions that explicitly models workload-dependent lead times.

We evaluate the performance of the different formulations under a wide range of operating conditions by simulating the execution of the corresponding production plans in a large-scale wafer fab. Our results show that the use of fractional lead times, when accurately estimated, yields substantial improvements in performance over that obtained using integer lead times. When total workload on the wafer fab remains stable over time, the models with fractional lead times yield results comparable to those from the clearing function model. When the system workload varies over time, workload-dependent lead times modeled by clearing functions outperform the remaining two approaches.

Efficient Algorithms in VLSI Routing

Sven Peyer
IBM
Schoenaicher Str. 220, 71032 Boeblingen, Germany
e-mail: sven.peyer@de.ibm.com

Routing is one of the most critical steps in VLSI design. Its main task is to find disjoint networks on the chip at the presence of numerous constraints. Often, several millions of connections need to be found in a short runtime. Due to this high complexity, routing is usually divided into two major steps: Global routing and detailed routing. For each network, global routing defines a search space in which detailed routing searches for a shortest path.

After an introduction to the routing problem we present main mathematical concepts to solve the global and detailed routing problems. These approaches have been applied for many years in IBM's routing solution in closed collaboration with the Research Institute for Discrete Mathematics at the University of Bonn, Germany. The talk closes with a discussion of challenges in advanced technology nodes.

Optimization in Product Design and Development

Monica Rafaila
Infineon Technologies
Am Campeon 1-12, Neubiberg, 85579 Germany
e-mail: rafaila.external@infneon.com

The presentation will give an overview of experiment planning and data analysis methods, as applied for application-oriented verification of electronic control units. The methods must find a trade-off between a reduced number of simulations and an accurate coverage highly-dimensional verification spaces. Another challenge is how to represent the results in an intuitive way, in order to correctly interpret higher order effects. Examples range from chip-level verification of technological variations, to application-oriented verification of a window-lift system in an automotive application.

Modeling and Solving Master Planning Problems in Semiconductor Manufacturing

Thomas Ponsignon
Infineon Technologies AG
Am Campeon 1-12, 85579 Neubiberg, Germany
e-mail: thomas.ponsignon@infineon.com

This talk deals with mid-term production planning problems, i.e. master planning, that arise in semiconductor manufacturing. In a first step, the Infineon master planning process activities are shown. Gaining better understanding, the surrounding processes, i.e. order management, are described. For improving the production planning results, possible heuristic and linear optimization methods, are proposed. The performance of two of these models is assessed and the results will be discussed. Additionally, the advantages and disadvantages of using different optimization methods should be identified. Moreover they should show, that today a choice between optimization, model size and result availability has to be done. This also influences Infineons future vision on what optimization method to use in the production planning process.

Transistor-Level Layout of CMOS Cells

Stefan Hougardy, Jan Schneider and Jannik Silvanus
Research Institute for Discrete Mathematics, University of Bonn
Lennestr. 2, 53113 Bonn, Germany
e-mail: hougardy,schneid,silvanus@or.uni-bonn.de

Modern computer chips consist of several billion transistors. In order to handle so many objects efficiently when designing such chips, several levels of hierarchy are introduced. On the lowest level of hierarchy, the layout of "leaf cells", only a small number of transistors need to be arranged and connected as area-efficient as possible. While one can hope for optimal solutions in some sense due to the small problem size, many difficult constraints have to be considered which are irrelevant in traditional placement and routing problems. For example, placement objects, namely the transistors, are allowed to overlap in specific situations and have a flexible aspect ratio, and the routing module must be aware of complicated constraints imposed on the geometry of the wires.

In this talk, we present a number of combinatorial problems arising in transistor-level VLSI layout and our approach to solve them using combinatorial algorithms and a routing formulation based on a mixed integer linear programming. An implementation of these algorithms, BonnCell, is currently in practical use for the automatic generation of full leaf cell layouts at our industry partner IBM.

Transport Modules with Two Independent Arms in Cluster Tools

Daniel Tonke
Technical University Munich
Arcisstr. 21, 80333 Munich, Germany
e-mail: daniel.tonke@tum.de

Recently, cluster tool robot systems with two independently operating robot arms have appeared on the industrial robotics market. Tool engineers believe that robots with independent arms can improve throughput. Accordingly, it is necessary to examine under which circumstances and to which extent productivity gains can be realized using such tools. Therefore, we examine a wafer handling robot with two independently moving robot arms inside a radial configuration cluster tool. For this architecture, we develop a Petri net model which represents the tool behavior. We show that the well-known swap sequence is not always the optimal sequence. Instead, we identify three other dominant types of sequences. Moreover, we develop a mixed integer programming formulation (MIP) to determine optimal sequences among 1-cyclic schedules. The MIP formulation can additionally be used to minimize the cycle time with consideration of wafer delay constraints. Furthermore, we analyze and demonstrate how the new tool architecture can increase throughput in comparison to the regular dual armed robot design. Finally, stochasticity in cluster tool scheduling is discussed.

Kombinierte Warteschlangen- und Optimierungsmodelle für die Planung in der Halbleiterfertigung

Horst Zisgen
IBM Deutschland, TPC Software Development
Hechtsheimer Str. 2, 55131 Mainz, Germany
e-mail: horst_zisgen@de.ibm.com

Die Fertigungsprozesse in der Halbleiterindustrie sind nicht nur technologisch höchst anspruchsvoll, sie sind auch hinsichtlich der Materialflüsse innerhalb der Fabrik äußerst komplex und stellen dadurch besondere Anforderungen an die Planung von Kapazitäten und Durchlaufzeiten. Angesichts der sehr hohen Investitionssummen für neue Fertigungskapazitäten und den mit den kurzen Lebenszyklen einhergehenden Zeitdruck als erster eine neue Technologie auf den Markt zu bringen, ist aber gerade eine zuverlässige und schnelle Planung für die Halbleiterfertiger essentiell.

Im diesem Vortrag wird zum einen ein Warteschlangennetzwerk vorgestellt, dass als Grundmodell für den Fertigungsprozess dient. Dabei wird aufgezeigt, wie die verschiedenen Maschinentypen über geeignete Warteschlangensysteme modelliert und in einem Netzwerk, als Modell für die gesamte Fabrikation, integriert werden können. Zum anderen wird ein Optimierungsmodell vorgestellt, mit dessen Hilfe sich das Routing der einzelnen Produkte und die Maschinenbelegung im Sinne einer verbesserten Durchlaufzeit und eines höheren Produktionsausstoes in Abhängigkeit eines sich veränderten Produktmixes optimieren lässt und wie dieses Optimierungsmodell in das Warteschlangennetzwerk integriert werden kann. Anhand von realen Fallbeispielen wird schließlich gezeigt, welchen praktischen Nutzen und finanziellen Vorteil diese Methoden im Einsatz erzielen können.